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1 Introduction

1.1 Overview

The 586F62T is a quality, high performance, function enhanced mainboard based on the Pentium class processor. This mainboard is designed around the latest and fastest Intel 82430HX chipset in a 3/4 baby AT form factor.

The 586F62T mainboard delivers superior performance with its integrated Bus Mastering EIDE (Enhanced IDE) controller, concurrent PCI bus, 256/512KB level 2 Pipelined Burst cache, and its ability to accommodate new technology EDO (Extended Data Out) DRAM.

The 586F62T mainboard achieves the highest reliability by supporting the ECC (Error Checking and Correction) memory protection on the data bus. This enables the 586F62T mainboard to have superior data integrity and be fault-tolerant in respect to memory errors while running applications.

The 586F62T mainboard offers outstanding I/O capabilities. It contains a full set of PC I/O such as dual channel PCI EIDE interfaces, a floppy controller, two FIFOed serial ports, an EPP/ECP capable bidirectional parallel port, an IrDA compatible infrared port, two USB (Universal Serial Bus) ports, and a PS/2 mouse port.Three PCI local bus slots and four full length ISA bus slots provide expandability to add on peripheral cards.

In addition to superior hardware capabilities, features like bus mastering EIDE driver, Plug and Play, APM (Advanced Power Management), and BIOS upgradability are provided on the 586F62T platform.

1.2 586F62T Specifications/Features

Hardware

CPU	Supports the following CPUs in a ZIF Socket 7 Intel Pentium P54C/P54CT/P54CTB/P55C - 75/90/100/120/133/150/166/180/200 MHz Cyrix 6x86/6x86L - P120/P133/P150/P166 AMD K5/K6
Coprocessor	CPU built-in floating point unit
Speed	System bus clock 50/55/60/66 MHz PCI bus clock 25/27.5/30/33 MHz ISA bus clock 7.5/8.33/9.15 MHz
Chipset	Intel's 82430HX PCIset Winbond's 83877 I/O chip
L2 Cache	Pipelined Burst SRAM 256/512KB
DRAM	4 x 72-pin SIMM sockets. Supports 8MB to 512MB memory Supports FPM and EDO DRAMs. Supports Parity/ECC memory protection.
EIDE Controller	Supports four IDE devices in two channels Supports PIO mode 0 through mode 4 drives Supports Bus Mastering DMA mode 2 drives
Enhanced I/O	One floppy disk controller One Standard/EPP/ECP bidirectional parallel port Two 16550 compatible high speed serial ports One IrDA compatible Infrared port Two USB (Universal Serial Bus) ports
Mouse/Keyboard	PS/2 mouse port AT keyboard connector
Expansion Slots	Three 32-bit PCI slots Four 16-bit ISA slots

Options	External Infrared port cable with mounting bracket External PS/2 Mouse cable with mounting bracket External dual USB ports cable with mounting bracket

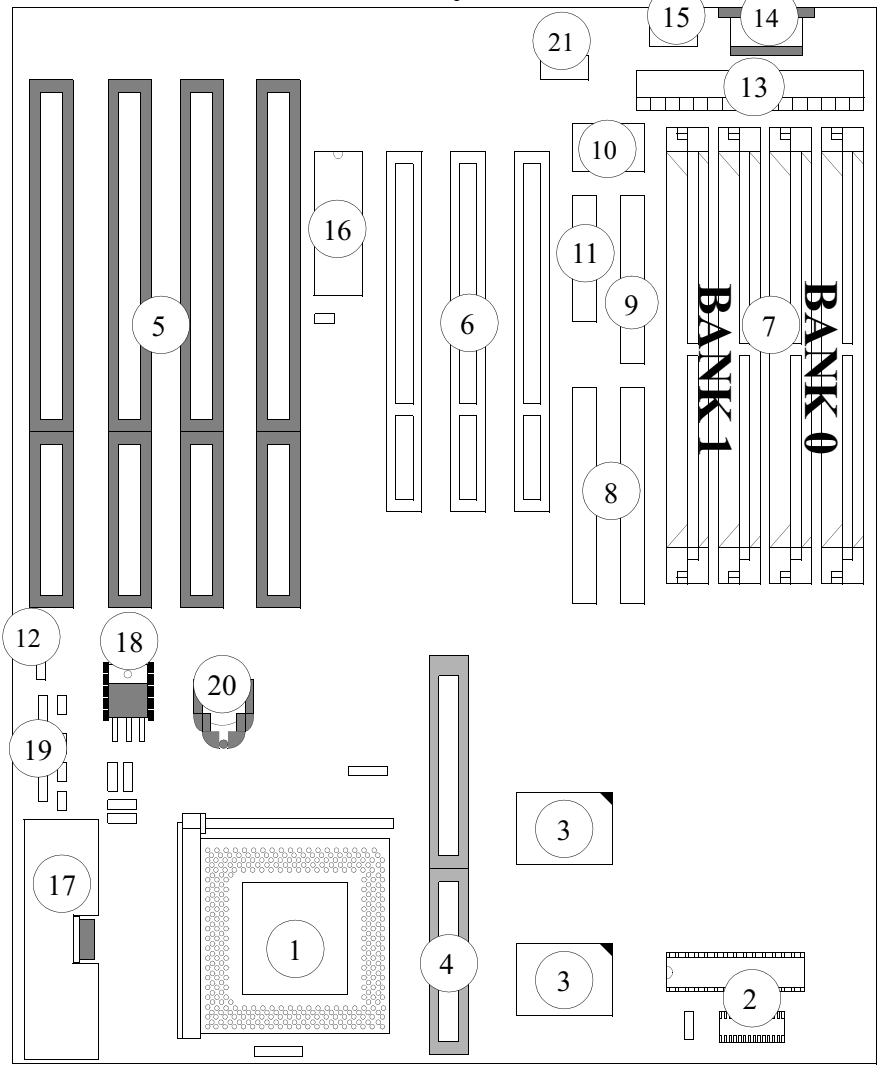
Software

BIOS	AWARD Pentium PCI BIOS Flash BIOS with ESCD (Extended System Configuration Data) block Supports APM, PnP, and EIDE devices Built-in NCR SCSI BIOS
Driver	Bus mastering EIDE driver
Utility	Flash utility for BIOS upgrade
O.S.	Operates with MS_DOS, Windows 3.x, Windows for Work Groups 3.x, Windows 95, Windows NT, OS/2, Novell Netware, Novell UnixWare 1.1 and SCO Unix 4.2

Environment

Ambient Temperature	0 to 50 C (Operating)
Relative Humidity	0 to 85% (Operating)
Vibration	0 to 500 Hz
DC Voltage	4.9V to 5.2V
DC Voltage	-5V, +12V, -12V, 5% tolerance

1.3 586F62T Mainboard Layout



1: CPU
2: TAG SRAM Chip
3: Cache SRAM Chips
4: Cache Slot
5: ISA Expansion Slots
6: PCI Expansion Slots
7: SIMM Module Sockets
8: IDE Connectors
9: Floppy Drive Connector
10: Serial Port Connectors
11: Paralle Port Connector
12: IR Port Connector
13: Power Connector
14: Keyboard Connector
15: PS/2 Mouse Header
16: BIOS ROM
17: CPU Core Voltage Regulator
18: I/O Voltage Regulator
19: Front panel Connectors
20: Battery (CR2032 Lithium)
21: USB Header

1.4 Microprocessor

The 586F62T mainboard is a flexible mainboard which is designed to operate with the Pentium class processors: Intel P54C (Pentium), P54CT (Pentium OverDrive), P54CTB (Pentium OverDrive with MMX Technology), and P55C (Pentium with MMX Technology), Cyrix 6x86 and 6x86L, and AMD K5 and K6.The 586F62T meets the requirements of a Pentium flexible mainboard. A Pentium flexible mainboard is defined as a mainboard capable to support all members of the Pentium class processors.

The requirements for a Pentium flexible mainboard are:

1. CPU ZIF socket is Socket 7.
2. BIOS can supports various Pentium class processors with different CPU core frequency.
3. On-board two voltage regulators and heat sinks meet CPU's core and I/O voltage/current/thermal specifications.

A cooling fan and heat sink assembly is required to protect the CPU from being damaged due to overheat.

1.5 Level 2 Cache

The 586F62T mainboard provides standard 256KB synchronous pipelined SRAM cache on board. To upgrade the cache size to 512KB, you can install a 256KB cache module onto the on-board cache slot.

1.6 Chipset

The Intel 82430HX PCIset consists of one 82439HX Xcellerated Controller (TXC), and one 82371SB PCI ISA/IDE Accelerator (PIIX3).

82439HX (TXC):
- CPU interface controller
- Cache and DRAM controllers
- DRAM Parity and Error checking /Correction.
- Fully synchronous PCI bus interface.

	- Extensive CPU-to-DRAM, PCI-to-DRAM and CPU-to-PCI data buffering
82371SB (PIIX3):	- Interface between the PCI and ISA buses - USB controller - EIDE controller - Seven DMA channels, one timer/ counter, two eight-channel interrupt controllers, NMI logic, SMI interrupt logic, and PCI/ISA bus arbitrator.

1.7 Main Memory

The 586F62T mainboard provides four 72-pin SIMM sockets to support 8MB to 512MB of system memory. The sockets support 1M x 32/36 (4MB), 2M x 32/36 (8MB), 4M x 32/36 (16MB), 8M x 32/36 (32MB) single- or double-sided modules.

The 586F62T supports two types of DRAMs, Fast Page Mode (FPM) and Extended Data Out (EDO). Memory Timing requires 70ns or faster.

Both parity and non-parity as well as ECC (Error Checking and Correction) are supported. The ECC is a hardware scheme used to achieve superior system main memory data integrity. The ECC detects all single and dual-bit errors, and corrects all single-bit error during main memory access. The Parity scheme can only do single-bit error detection. The ECC or Parity can only be supported properly if all DRAMs are 72-bit wide (by 36).

The four SIMM sockets are divided into two banks of two sockets each. The sockets are designated Bank 0 and Bank 1. Each bank provides a 64-bit non-parity or 72-bit parity/ECC data path. **Both SIMMs in a bank must be of the same memory size, type and speed.** There are no jumper settings required for the memory size or type, which is automatically detected by the BIOS.

EDO DRAM is designed to improve the DRAM read performance. It holds the memory data valid until the next memory access cycle, unlike FPM DRAM that tri-states the memory data when the precharge cycle occurs, prior to the next memory access cycle.

1.8 Enhanced IDE Support

The586F62T mainboard provides two enhanced high performance PCI IDE interfaces capable of supporting four PIO mode 0 through mode 4 and bus-mastering DMA mode 2 ATAPI devices. Detection of IDE device type and transfer rate (PIO mode) is automatically determined by the BIOS.

The traditional PIO IDE requires a substantial amount of CPU bandwidth to handle all the activities of IDE access including waiting for mechanical activity. The Bus Master logic designed in the Intel 82430HX chipset is intended to reduce the workload of the CPU, and to increase CPU efficiency. The Bus Master will take care of the data transfer between IDE and memory and let the CPU handle other tasks. In true multi-tasking operating systems such as Windows 95, Windows NT, and OS/2, by using bus-mastering IDE, the CPU bandwidth can be freed up to complete other tasks while disk data transfers are occurring. In order to make the EIDE drive operate at bus-mastering DMA mode 2, the driver must be loaded properly.

1.9 Universal Serial Bus Support

The 586F62T provides two USB ports. The USB is a serial bus interface standard that is designed to bring the “Plug and Play” concept to the outside of the computer system chassis. The bus allows devices to be attached, configured, used and also detached while the host system is in operation.

The USB will allow as many as 63 devices to be daisy chained in any combination per port. Up to 12Mbits/sec transfer rate, makes it suitable for devices such as keyboard, mouse, digital joystick, game pad, fax/modem, scanner, printer, ISDN and telephony device.

1.10 Real-time Clock, CMOS RAM and Battery

The integrated real-time clock (RTC) provides a time of day clock, 100-year calendar with alarm features. The RTC also has 242 bytes battery backed CMOS RAM which stores the system setup information and password. The RTC and CMOS RAM can be set via the BIOS SETUP program. The content of the CMOS RAM can be cleared by placing a shunt to short pin1 and pin2 of JP2 for 5 seconds when the system power is off.

An external coin-cell style Lithium CR2302 battery is used to provide power to the RTC and CMOS memory. The battery has three years lifetime if the system does not power up. When the system powers up, the power for the RTC and CMOS RAM is supplied from the 5 V power supply to extend the life of the battery.

1.11 IrDA Infra-red Support

A 5-pin header connector is used to connect a Hewlett Packard HSDSL-1000 compatible IrDA Infrared module. Once the module is installed, the user can use application software such as Laplink to transfer files between the computer system and portable devices such as laptops and printers. The Serial port 2 must be configured to support an IrDA module via the BIOS SETUP program.

2 Hardware Installation

2.1 Unpacking

The 586F62T mainboard package contains the following:

* 586F62T mainboard
* One IDE 40-pin ribbon cable
* One floppy 34-pin ribbon cable
* Two serial ports cable with mounting bracket
* One parallel port cable with mounting bracket
* User's manual

Before removing the mainboard from its anti-static bag, you need to eliminate any static electricity that may be accumulated on your body by touching a grounded or anti-static surface. If nothing is available, touch the housing of the power supply which is plugged into the AC outlet.

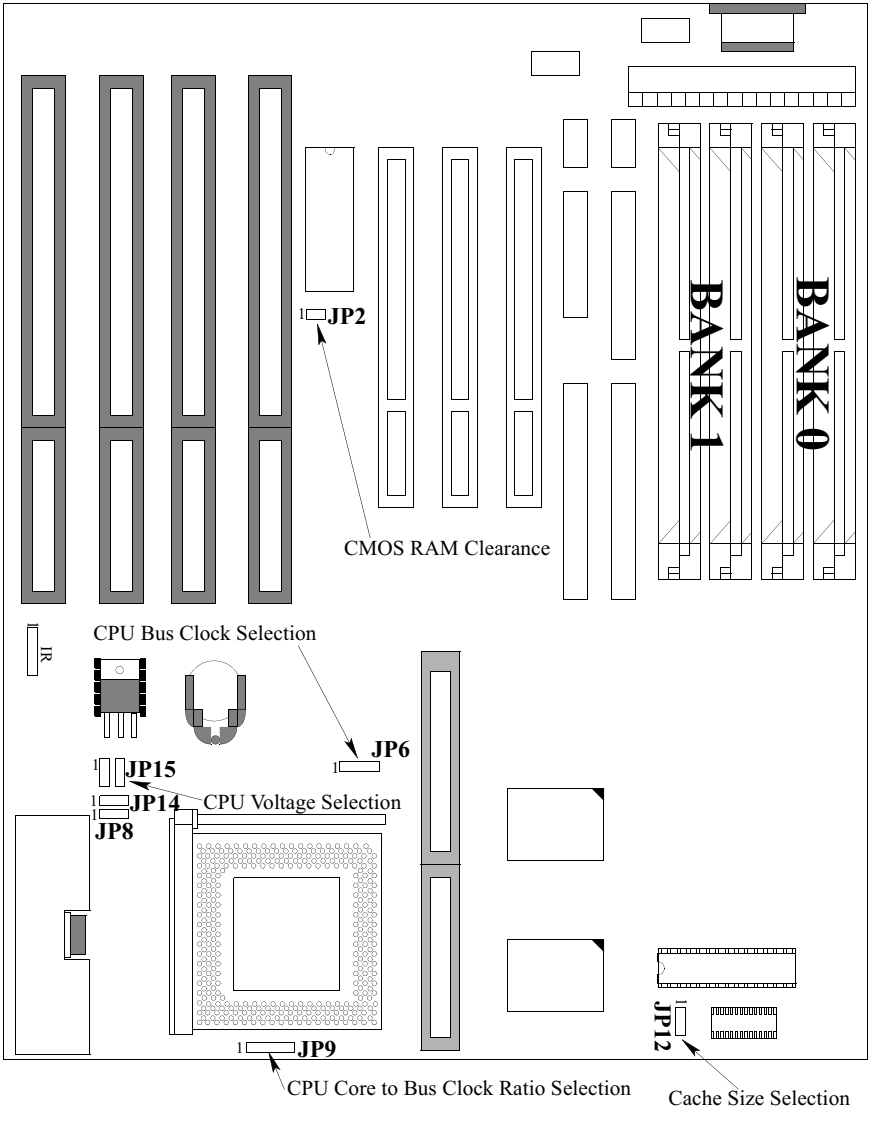
After removing the mainboard from its anti-static bag, place it only on a grounded or anti-static surface, component side up. Inspect the mainboard to see if it is damaged, call the vendor immediately if it is damaged.

2.2 Installation

The 586F62T is designed to fit into a standard AT form factor chassis. The pattern of the mounting holes and the position of the back panel connectors match the AT system board specification. Chassis may come with various mounting fasteners which are made of metal or plastic. It is highly recommended to use as many metal fasteners as possible to mount the mainboard in the chassis for better grounding.

To install the mainboard you need to set jumpers, attach connectors, install CPU and SIMM memory modules.

586F62T Mainboard Jumper Location

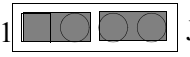
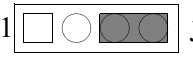
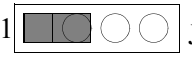


2.2.1 Setting Jumpers

CPU Bus Clock Selection (JP6)

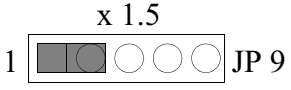
This jumper selects different CPU Bus Clock

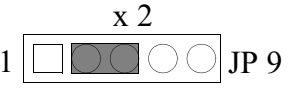
.

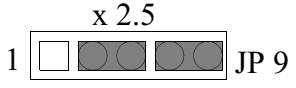
CPU Bus Clock	PCI Bus Colck	ISA Bus Colck	Jumper Setting JP6
50MHz	25MHz	8.33MHz	
55MHz	27.5MHz	9.16MHz	
60MHz	30MHz	7.5MHz	
66.6MHz	33.3MHz	8.33MHz	

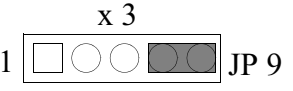
CPU Core to Bus Clock Ratio Selection (JP9)

This jumper selects different CPU core to bus clock ratio.





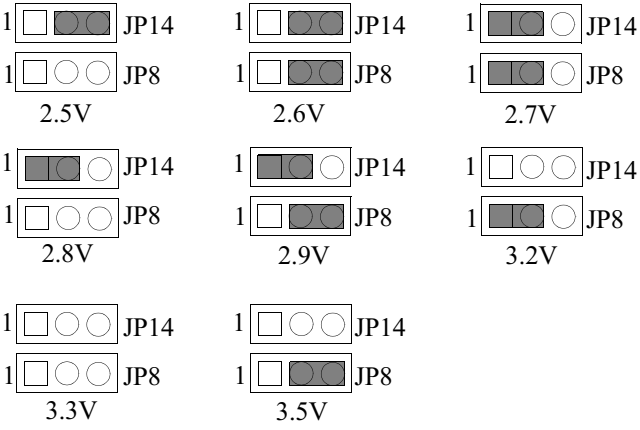




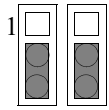
The actual core frequentness be found by multiplying the CPU bus clock frequency by Core/Bus multiplier. For example, if the CPU bus clock freqency is 66.6MHz and the Core/Bus multiplier is 3, the actual CPU core frequency will be 66.6 x 3 = 200MHz.

. CPU Voltage Selection

These jumpers select different voltages for the CPU.



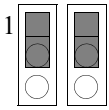
CPU Core Voltage = I/O Voltage



Single Operating Voltage CPUs

- Intel P54C/P54CT/P54CTB
- Cyrix 6x86
- AMD K5

CPU Core Voltage ≠ I/O Voltage

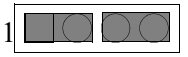
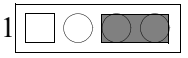
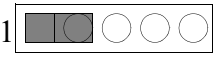
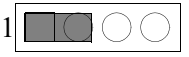
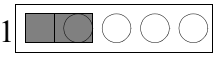
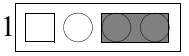
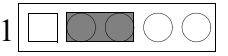
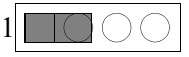
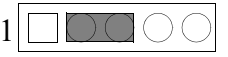
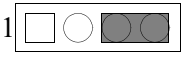
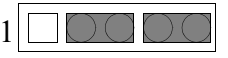
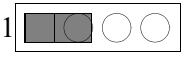
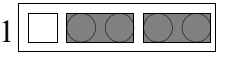
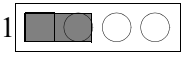
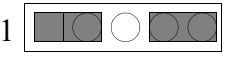


Dual Operating Voltage CPUs

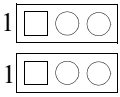
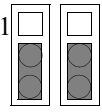
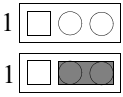
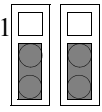
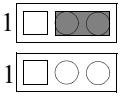
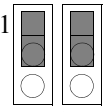
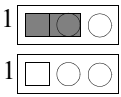
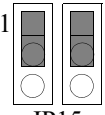
- Intel P55C
- Cyrix 6x86L & M2
- AMD K5 - PRxx xHx

Intel Pentium CPU clock jumper setting

Intel Pentium CPU Click jumper setting

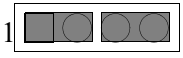
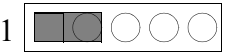
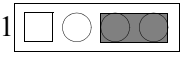
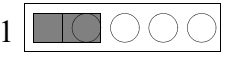
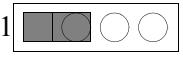
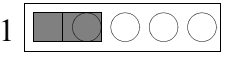
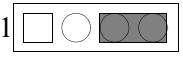
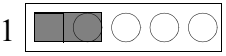
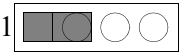
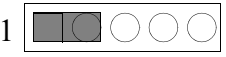
CPU Speed	JP6	JP9
Pentium -75 50MHz x 1.5		
Pentium -90 60MHz x1.5		
Pentium -100 66MHz x 1.5		
Pentium - 120 60MHz x 2		
Pentium -133 66MHz x 2		
Pentium - 150 60MHx x 2.5		
Pentium -166 66MHz x 2.5		
Pentium -200 66MHz x 3		

Intel Pentium CPU voltage jumper setting

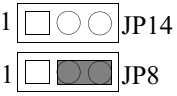
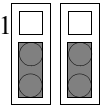
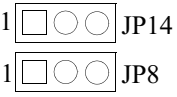
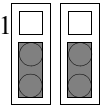
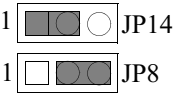
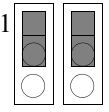
CPU Voltage (Volts)	JP14 JP8	JP15
3.3 V		
3.5 V		
3.3 V I/O 2.5 V Core (P55C)		
3.3 V I/O 2.8 V Core (P55C)		

AMD CPU Clock/Voltage Jumper Setting

AMD CPU Clock Jumper Setting

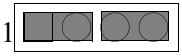
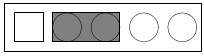
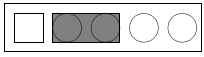
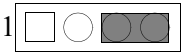
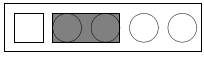
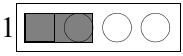
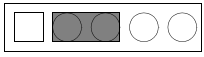
CPU Speed	JP6	JP9
AMD-K5-PR75 50MHz x 1.5		
AMD-K5-PR90 60MHz x1.5		
AMD-K5-PR100 66MHz x 1.5		
AMD-K5-PR120 60MHz x 1.5		
AMD-K5-PR133 66MHz x 1.5		

AMD CPU voltage jumper setting

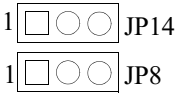
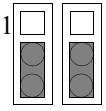
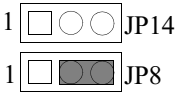
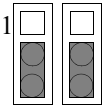
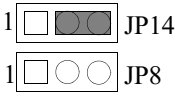
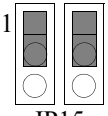
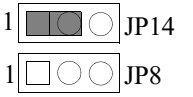
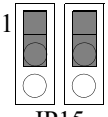
CPU Voltage (Volts)	JP11 JP12	JP13 JP14
3.5 V AMD-K5-PRxx xBx		
3.3 V AMD-K5-PRxx xFx		
3.3 V I/O 2.92 V Core AMD-K5-PRxx xHx		

Cyrix 6x86 CPU Clock/Voltage Jumper Setting

Cyrix 6x86 CPU clock jumper setting

CPU Speed	JP6	JP9
Cyrix 6x86 - P120+ 100MHZ = 50 x 2		
Cyrix 6x86 - P133+ 110MHz = 55 x 2		
Cyrix 6x86 - P150+ 120MHz = 60 x 2		
Cyrix 6x86 - P166+ 133MHz = 66 x 2		

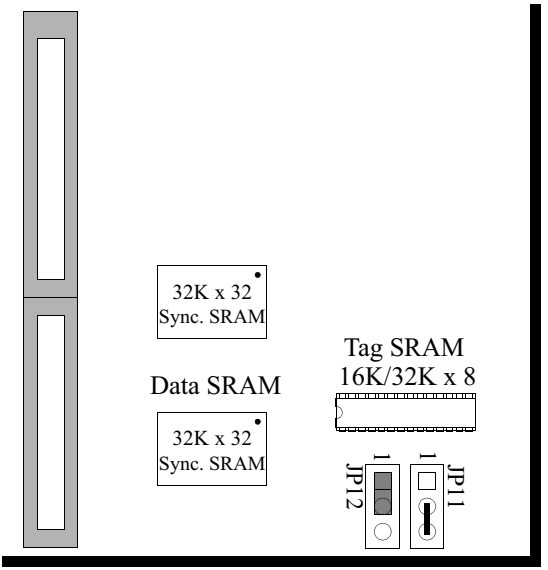
Cyrix 6x86 CPU voltage jumper setting

CPU Voltage (Volts)	JP14 JP8	JP15
3.3 V		
3.5 V		
3.3 V I/O 2.5 V Core (6x86L)		
3.3 V I/O 2.8 V Core (6x86L, M2)		

Cache Memory Selection

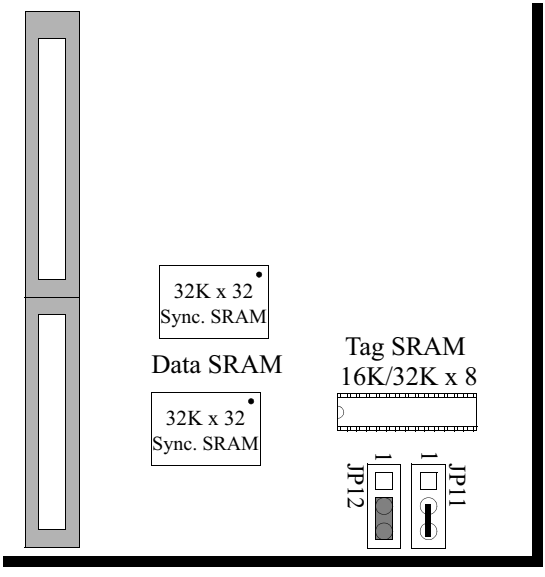
The 586F62T Mainboard supports Synchronous SRAMs on board and/or Cache module in the Cache Slot. The 586F62T has two cache size options: 256KB or 512KB. The figures below show jumper setting for each configuration.

(1) 256KB Cache On Board

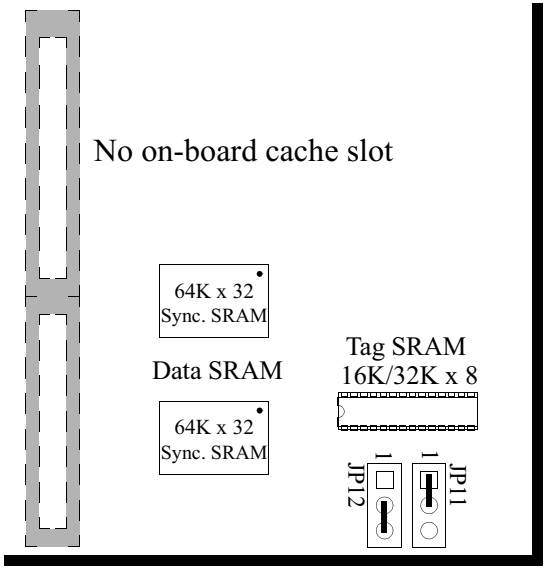


(2) 256KB Cache On Board and 256KB Cache Module, Total 512KB

Note: Only Cache Module designed following Intel COAST specification will work in this configuration.



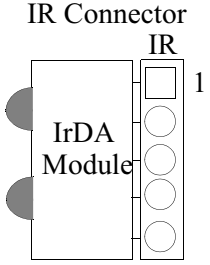
(3) 512KB Cache On Board



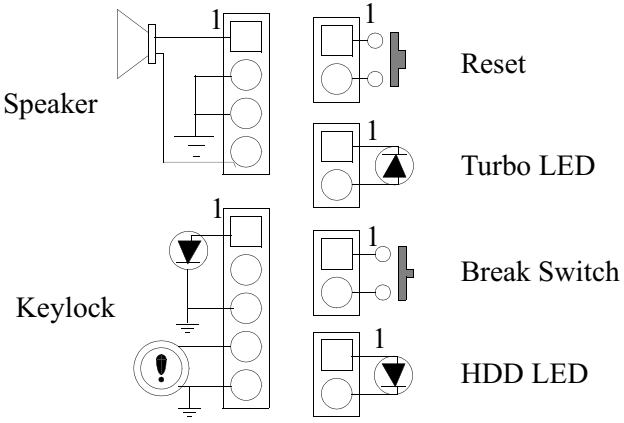
2.2.2 Attaching Connectors

Front Panel Connectors

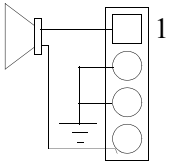
There are 7 connectors on the Mainboard for switches and indicator lights from the system front panel.



Pin Assignment
1. +5V
2. N. C.
3. IR Receiver
4. Ground
5. IR Transmitter

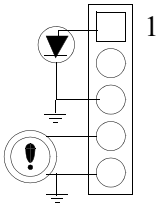


Speaker Connector



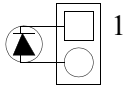
Pin Assignment
1. Speaker out
2. Ground
3. Ground
4. +5V

Keylock Connector



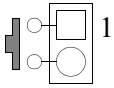
Pin Assignment
1. LED Cathode
2. N. C.
3. LED Anode (Ground)
4. Keylock
5. Ground

HDD LED Connector



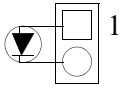
Pin Assignment
1. LED Anode
2. LED Cathode

Reset Connector



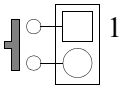
Pin Assignment
1. Power Good
2. Ground

Turbo LED Connector



Pin Assignment
1. LED Cathode
2. LED Anode (Ground)

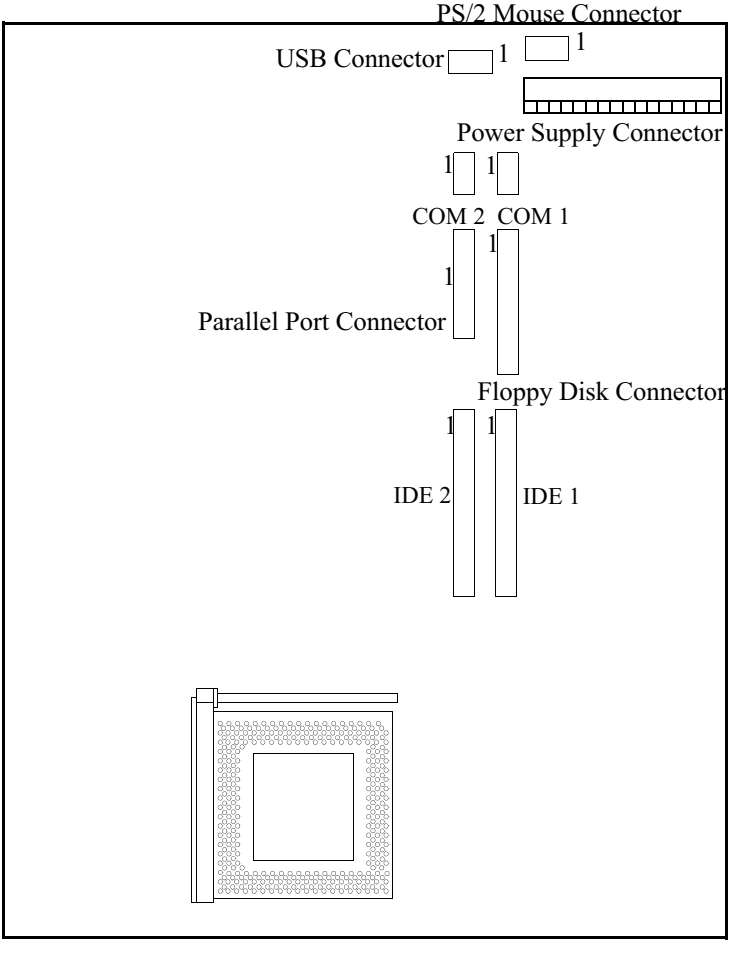
Break Switch Connector



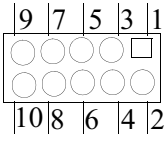
Pin Assignment
1. Break
2. Ground

The front panel on your case may have a turbo switch to deactivate the Turbo mode when a slower speed is required for a specific application. The Intel 82430HX chipset does not support the hardware deturbo function. An alternative method of using <CTRL><ALT><+/-> keys to change the speed may be used if necessary.

I/O Port Connectors



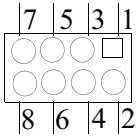
USB Connector



Pin Assignment

1. +5V	2. +5V
3. USB D0-	4. USB D1-
5. USB D0+	6. USB D1+
7. Ground	8. Ground
9. Ground	10. Ground

PS/2 Mouse Connector



Pin Assignment

1. +5V	2. N.C.
3. N.C.	4. N.C.
5. MSDATA	6. N.C.
7. Ground	8. MSCLK

Use the following information to connect the floppy disk drives, IDE drives, and USB cable.

1. You must orient the cable connector so that the pin 1(color) edge of the cable is at the pin 1 of the I/O port connector.

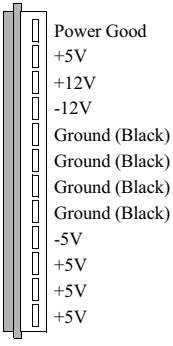
2. A floppy disk drive ribbon cable has 34 wires and 2 connectors to support 2 floppy disk drives. The connector with twisted wires always connects to drive A, and the connector which does not have twisted wire connects to drive B.

3. An IDE drive ribbon cable has 40 wires and 2 connectors to support two IDE drives. If a ribbon cable connects to two IDE drives at the same time, one of them has to be configured as Master and the other one has to be configured as Slave by setting the drive select jumpers on the drive. Consult the documentation that comes with your IDE drive for details on jumper locations and settings.

Power Supply Connector

Incorrect installation of the power supply could result in serious damage to the mainboard and connected peripherals. Make sure the power supply is unplugged before connecting the leads from the power supply.

AT Power Connector



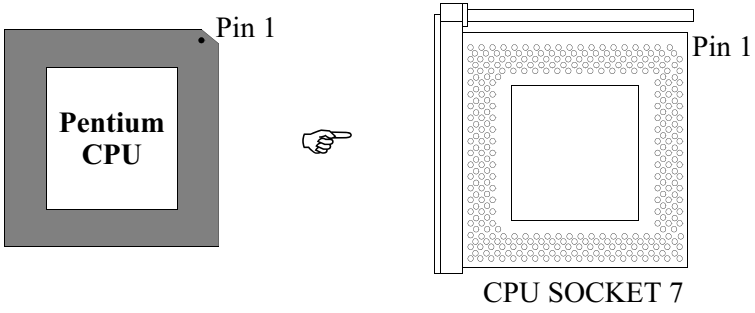
Most AT power supplies have two leads. Each lead has six wires, two of which are black.

Orient the leads so the black wires are along side each other, making the black wires plug in the middle of the connector. Align the plastic guide pins on the lead cables with the connector on the mainboard. Press the lead connector so that its plastic clips snap into place and secure the leads in the connector.

2.2.3 Installing CPU

To avoid being broken by the pressure of CPU insertion, the mainboard must be placed on a flat anti-static surface before the CPU is installed. Do not touch the CPU pins with your fingers during the installation.

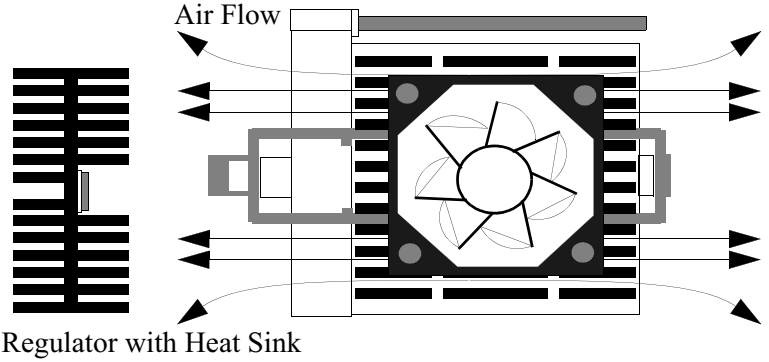
1. Push the CPU ZIF socket's lever to the side a little and raise it as far as it can go.
2. Align the CPU with the ZIF Socket 8 so that the pin 1 (cut corner) of CPU is at the pin 1 of the Socket 7 as shown in the figure below, then insert the CPU into the socket.
3. Press the lever down to snap it into place at the side of socket. You will feel some resistance as the pressure starts to secure the CPU in the socket.
4. Install a heatsink with a cooling fan that is required to protect the CPU from being damaged due to overheat.



2.2.4 Tips for Cyrix CPU Installation

1. Cyrix CPU package includes: Cyrix CPU, Thermalloy (a piece of alloy + Thermal Grease), Heat sink with a fan.
2. Follow the instructions in section 2.2.3 to install the Cyrix CPU onto the CPU socket.
3. Apply Thermalloy on top of the CPU Heat Spreader. Most heat sinks are not perfectly flat, the air gap need to be filled with an interface material that has a lower thermal resistance than air.
4. To gain more efficient heat removal, place the CPU heat sink with it's grid stripes toward the Regulator heat sink (see the drawing below). This geometric position will increase air flow blowing toward the regulator heat sink and gain more efficient heat removal.

   However, the original Cyrix CPU heat sink does not have the right geometric position. You need to simply modify it. Use the flat screw driver to detach the fan from the heat sink, place the clip metal in the middle along the grid's direction. Attach back the fan and press gently two adjacent corners until the clip snap to the grid.

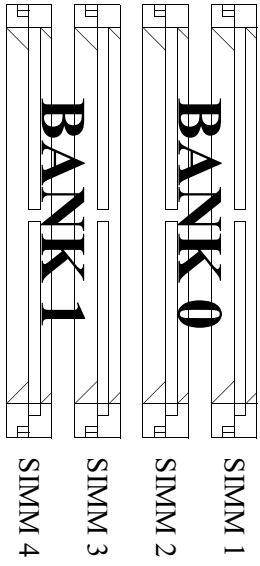


After Modification

2.2.5 Installing System Memory

The 586F62T Mainboard has four SIMM Sockets to support up to 512MB of system memory. The four SIMM sockets (SIMM1 ~ SIMM4) are divided into 2 Banks, Bank0 (SIMM1, SIMM2) and Bank1 (SIMM3, SIMM4).

Memory can be installed by using 72-pin EDO or Fast Page Mode SIMM memory modules. Due to the 586F62T Mainboard high speed design, the memory modules for the 586F62T must meet all of following requirements:



DRAM TYPE	EDO (Extended Data Output) FPM (Fast Page Mode)	
DATA INTEGRITY	None	Supports ECC/Parity
MODULED SIZE	**Single-sided** Symmetric : 1Mx32 4Mx32 16Mx32 Asymmetric: 521Kx32 1Mx32 2Mx32 4Mx32 8Mx32 **Double-sided** Symmetric : 2Mx32 8Mx32 32Mx32 Asymmetric: 1Mx32 2Mx32 4Mx32 8Mx32 16Mx32	**Single-sided** Symmetric : 1Mx36 4Mx36 16Mx36 Asymmetric: 521Kx36 1Mx36 2Mx36 4Mx36 8Mx36 **Double-sided** Symmetric : 2Mx36 8Mx36 32Mx36 Asymmetric: 1Mx36 2Mx36 4Mx36 8Mx36 16Mx36
REQUIREMENTS	DRAM Speed : 60ns or 70ns RAS Access Time : 60ns ~ 70ns CAS Access Time : 10ns ~ 25ns Two SIMM modules must be installed at a time and each pair of modules must be the same size, type and speed.	

The following table shows the system memory configuration which **does not** support ECC/Parity feature.

BANK 0	BANK 1
EDO/FPM, Two 72-pin SIMM modules	EDO/FPM, Two 72-pin SIMM modules
None **Single-sided** Symmetric : 1Mx32, 4Mx32, 16Mx32 Asymmetric: 512Kx32, 1Mx32, 2Mx32, 4Mx32, 8Mx32	**None** **Single-sided** Symmetric : 1Mx32, 4Mx32, 16Mx32 Asymmetric: 512Kx32, 1Mx32, 2Mx32, 4Mx32, 8Mx32
None **Single-sided** Symmetric : 1Mx32, 4Mx32, 16Mx32 Asymmetric: 512Kx32, 1Mx32, 2Mx32, 4Mx32, 8Mx32	**None** **Double-sided** Symmetric : 2Mx32, 8Mx32, 32Mx32 Asymmetric: 1Mx32, 2Mx32, 4Mx32, 8Mx32, 16Mx32
None **Double-sided** Symmetric : 2Mx32, 8Mx32, 32Mx32 Asymmetric: 1Mx32, 2Mx32, 4Mx32, 8Mx32, 16Mx32	**None** **Single-sided** Symmetric : 1Mx32, 4Mx32, 16Mx32 Asymmetric: 512Kx32, 1Mx32, 2Mx32, 4Mx32, 8Mx32
None **Double-sided** Symmetric : 2Mx32, 8Mx32, 32Mx32 Asymmetric: 1Mx32, 2Mx32, 4Mx32, 8Mx32, 16Mx32	**None** **Double-sided** Symmetric : 2Mx32, 8Mx32, 32Mx32 Asymmetric: 1Mx32, 2Mx32, 4Mx32, 8Mx32, 16Mx32

The following table shows the system memory configuration which supports ECC/Parity feature.

BANK 0	BANK 1
EDO/FPM, Two 72-pin SIMM modules	EDO/FPM, Two 72-pin SIMM modules
None **Single-sided** Symmetric : 1Mx36, 4Mx36, 16Mx36 Asymmetric: 512Kx36, 1Mx36, 2Mx36, 4Mx36, 8Mx36	**None** **Single-sided** Symmetric : 1Mx36, 4Mx36, 16Mx36 Asymmetric: 512Kx36, 1Mx36, 2Mx36, 4Mx36, 8Mx36
None **Single-sided** Symmetric : 1Mx36, 4Mx36, 16Mx36 Asymmetric: 512Kx36, 1Mx36, 2Mx36, 4Mx36, 8Mx36	**None** **Double-sided** Symmetric : 2Mx36, 8Mx36, 32Mx36 Asymmetric: 1Mx36, 2Mx36, 4Mx36, 8Mx36, 16Mx36
None **Double-sided** Symmetric : 2Mx36, 8Mx36, 32Mx36 Asymmetric: 1Mx36, 2Mx36, 4Mx36, 8Mx36, 16Mx36	**None** **Single-sided** Symmetric : 1Mx36, 4Mx36, 16Mx36 Asymmetric: 512Kx36, 1Mx36, 2Mx36, 4Mx36, 8Mx36
None **Double-sided** Symmetric : 2Mx36, 8Mx36, 32Mx36 Asymmetric: 1Mx36, 2Mx36, 4Mx36, 8Mx36, 16Mx36	**None** **Double-sided** Symmetric : 2Mx36, 8Mx36, 32Mx36 Asymmetric: 1Mx36, 2Mx36, 4Mx36, 8Mx36, 16Mx36

2.2.6 Clear CMOS and Password

If your system can not boot up because you forget your password, or the CMOS settings need to be reset to default values because the system BIOS is updated, the following instructions can be performed to clear the CMOS and password.

1. Power off the system
2. Place a shunt to short pin1 and pin2 of JP2 for 5 seconds
3. Remove the shunt
4. Power on the system

3 BIOS Configuration

After hardware configuration of 586F62T Mainboard is completed, and system hardware has been assembled, the completed system may be powered up. At this point, software setup should be run to ensure that system information is correct.

Normally, system setup is needed when the system hardware is not consistent with the information contained in the CMOS RAM, whenever the CMOS RAM has lost power, or the system features need to be changed.

3.1 Entering Setup

When the system is powered on, the BIOS will enter the Power-On Self Test (POST) routines. These routines perform various diagnostic checks at the time the system is powered up; if an error is encountered, the error will be reported in one of two different ways. If the error occurs before the display device is initialized, a series of beeps will be transmitted. If the error occurs after the display device is initialized, the screen will display the error message.

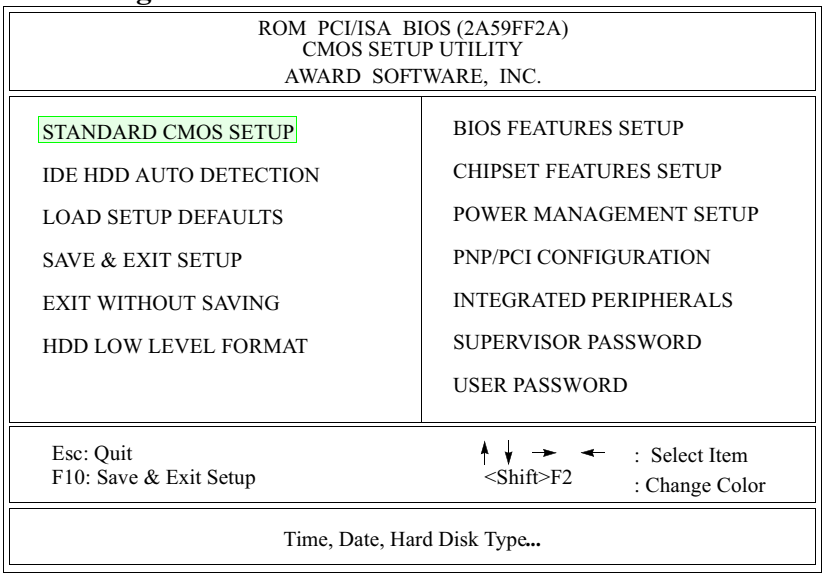
After the POST routines are completed, the following message appears:

"Press DEL to enter SETUP"

To access the AWARD BIOS SETUP program, press the <DEL> key. The "CMOS SETUP UTILITY" screen will be displayed at this time.

3.2 CMOS SETUP UTILITY

Main Program Screen



This screen provides access to the utility's various functions.

Listed below are explanations of the keys displayed at the bottom of the screen:

<ESC>: Exit the utility.

ARROW KEYS: Use arrow keys to move cursor to desired selection.

<F10>: Saves all changes made to Setup and exits program.

<Shift> <F2>: Changes background and foreground colors.

3.3 STANDARD CMOS SETUP

Selecting “STANDARD CMOS SETUP “on the main program screen displays this menu:

Standard CMOS Setup Screen

ROM PCI/ISA BIOS (2A59FF2A)
STANDARD CMOS SETUP
AWARD SOFTWARE, INC.

Date (mm:dd:yy): Mon, Feb 26 1996
Time (hh:mm:ss): 10:10:10

HARD DISKS	TYPE	SIZE	CYLS	HEAD	PRECOMP	LANDZ	SECTOR	MODE
Primary Master	: Auto	0	0	0	0	0	0	Auto
Primary Slave	: Auto	0	0	0	0	0	0	Auto
Secondary Master	: Auto	0	0	0	0	0	0	Auto
Secondary Slave	: Auto	0	0	0	0	0	0	Auto

Drive A : 1.44M, 3.5 in.
Drive B : None

Video : EGA/VGA
Halt On : All Errors

Base Memory : 640K
Extended Memory : 15360K
Other Memory : 384K

Total Memory : 16384K

ESC: Quit ↑ ↓ → ← : Select Item PU/PD/+/-:Modify
F1: Help (Shift) F2 : Change Color

The Standard CMOS Setup utility is used to configure the following features:

Set Date: Month, Date, Year.

Set Time: Hour, Minute, and Second. Use 24 Hour clock format (for PM numbers, add 12 to the hour, you would enter 4:30 p.m. as 16:30).

Hard Disks:
There are four hard disks listed: “Primary Master”, “Primary Slave”, “Secondary Master” and “Secondary Slave”. For Each

IDE channel, the first device is the “Master” and the second device is “Slave”.

Hard disk Types from 1 to 45 are standard ones; Type “Auto” is IDE HDD auto detection; Type “User” is user definable, and Type “None” is not installed (e.g. SCSI).

There are six categories of information you must enter for a HDD: “CYLS” (number of cylinders), “HEAD” (number of heads), “PRECOMP” (write pre-compensation), “LANDZ” (landing zone), “SECTOR” (number of sectors) and “MODE” (Normal, LBA, LARGE and AUTO). The hard disk vendor’s or system manufacturer’s documentation should provide you the information needed. For an IDE hard drive, you can set ‘TYPE’ to “Auto” or use the “IDE HDD AUTO DETECTION” utility in the main program screen to enter the drive specifications.

The AWARD BIOS supports three HDD modes: NORMAL, LBA and LARGE.

NORMAL mode: Generic access mode in which neither the BIOS nor the IDE controller will make any transformation during accessing. The maximum HDD size supported by the NORMAL mode is 528 Megabytes.

LBA mode: Logical Block Addressing mode is a HDD accessing method to overcome the 528Megabytes restriction. The number of cylinders, heads and sectors shown in setup may not be the number physically contained in the HDD.

During HDD accessing, the IDE controller will transform the logical address described by the cylinder, head and sector numbers into its own physical address inside the HDD. The maximum HDD size supported by the LBA mode is 8.4 Gigabytes.

LARGE mode: Some IDE HDD contains more than 1024 cylinders without LBA support. This access mode tricks DOS (or other OS) that the number of cylinders is less than 1024 by dividing it by 2. At the same time, number of heads is multiplied by 2.

A reverse transformation process will be made inside INT13h in order to accessing the right HDD address. The maximum HDD size supported by the LARGE mode is 1 Gigabytes.

Note: To support LBA or LARGE mode, there must be some software involved. All these software are located in the AWARD HDD Service Routine "INT13h". It may fail to access a HDD with LBA or LARGE modes selected if you are running under an Operating System which replaces the whole INT13h service routine.

Floppy Drive A and Floppy Drive B: The options are: "360K, 5.25 in.", "1.2M, 5.25in.", "720K, 3.5in.", "1.44M, 3.5in.", "2.88M, 3.5in." and "None (Not Installed)". Not Installed could be used as an option for diskless workstations.

3.4 IDE HDD AUTO DETECTION

If your system has an IDE hard drive, you can use this utility to detect its parameters and enter them into the Standard CMOS Setup automatically.

If the auto-detected parameters displayed do not match the ones that should be used for your hard drive, do not accept them. Press the <N> key to reject the values and enter the correct ones manually on the Standard CMOS Setup screen.

Note: If you are setting up a new hard disk drive (nothing on it) that supports LBA mode, more than one line will appear in the parameter box, choose the line that lists LBA for an LBA drive.

Do not choose Large or Normal if the hard disk drive is already fully formatted when you install it, choose the mode which is used to format it.

3.5 LOAD SETUP DEFAULTS

“LOAD SETUP DEFAULTS” loads optimal settings which are stored in the BIOS ROM.

The defaults loaded only affect the BIOS Features Setup, Chipset Features Setup, Power Management Setup, PnP/PCI configuration setup and Integrated Peripherals Setup.There is no effect on the Standard CMOS Setup. To use this feature, highlight on the main screen and press <Enter>. A line will appear on the screen asking if you want to load the Setup default values. Press the <Y> key and then press the <Enter> key if you want to load the Setup defaults. Press <N> if you don’t want to proceed.

3.6 SAVE & EXIT SETUP

Selecting this option and pressing the <Enter> key to save the new setting information in the CMOS memory and continue with the booting process.

3.7 EXIT WITHOUT SAVING

Selecting this option and pressing the <Enter> key to exit the Setup Utility without recording any new values or changing old ones.

3.8 HDD LOW LEVEL FORMAT

Selecting this option and pressing the <Enter> key enable you to perform low level format of hard disk drive.

3.9 BIOS FEATURES SETUP

Selecting “BIOS FEATURES SETUP” on the main program screen displays this menu:

BIOS Features Setup Screen

ROM PCI/ISA BIOS (2A59FF2A)
BIOS FEATURES SETUP
AWARD SOFTWARE, INC.

Virus Warning	: Disabled
CPU Internal Cache	: Enabled
External Cache	: Enabled
Quick Power On Self Test	: Disabled
Boot Sequence	: C, A
Swap Floppy Drive	: Disabled
Boot Up Floppy Seek	: Enabled
Boot Up NumLock Status	: On
Gate A20 Option	: Fast
Typematic Rate Setting	: Disabled
Typematic Rate (Chars/Sec)	: 6
Typematic Delay (Msec)	: 250
Security Option	: Setup
PCI/VGA Palette Snoop	: Disabled

Video BIOS Shadow	: Enabled
C8000 - CBFFF Shadow	: Disabled
CC000 - CFFFF Shadow	: Disabled
D0000 - D3FFF Shadow	: Disabled
D4000 - D7FFF Shadow	: Disabled
D8000 - DBFFF Shadow	: Disabled
DC000 - DFFFF Shadow	: Disabled
PS/2 mouse function control	: Disabled
OS Select For DRAM>64MB	: No-OS2

ESC : Quit ↑ ↓ → ← :Select Item
F1 : Help PU/PD/+/- :Modify
F5 : Old Values (Shift) F2: Color
F6 : Load BIOS Defaults
F7 : Load Setup Defaults

The following explains the options for each features:

Virus Warning: The Virus Warning’s default setting is “Disabled”. When enabled, any attempt to write the boot sector and partition table will halt the system and cause a warning message to appear. If this happens, you can use an anti-virus utility on a virus free, bootable floppy diskette to reboot and clean your system.

CPU Internal Cache: The default setting is “Enabled”. This Setting enables the CPU internal cache.

External Cache: The default setting is “Enabled”. This setting enables the external cache.

Quick Power On Self Test: The default setting is “Disabled”. If enabled, this will skip some diagnostic checks during the Power On Self Test (POST) to speed up booting process.

Boot Sequence: The default setting is “C,A”; the other option are “CDROM, C, A” and “C, CDROM, A”. The BIOS will load the operating system from the disk drives in the sequence selected here.

Swap Floppy Drive: The default setting is “Disabled”. This setting gives you an option to swap A and B floppy disks. Normally the floppy drive A is the one at the end of the cable, if you set this option to “Enabled”, the drive at the end of the cable will be swapped to B.

Boot Up Floppy Seek: The defaults setting is “Enabled”. When enabled, the BIOS will check whether there is a floppy disk drive installed.

Boot Up Numlock Status: The default setting is “On”. If set “Off”, the cursor controls will function on the numeric keypad.

Gate A20 Option: the defaults setting is “Fast”. This is the optimal setting for the Mainboard. The other option is “Normal”.

Typematic Rate Setting: The default setting is “Disabled”. If enabled, you can set the typematic Rate and typematic Delay.

Typematic Rate (Chars/Sec): This setting controls the speed at which the system registers repeated keystrokes. The choices range from 6 to 30 Chars/Sec. The default setting is “6” Chars/Sec.

Typematic Delay (Msec): This setting controls the time between the display of the first and second characters. There are four delay choices: 250ms, 500ms, 750ms and 1000ms. The default setting is "250" ms.

Security Option: This setting controls the password feature. The options are "Setup" and "System". Select "Setup" will protect the configuration settings from being tampered with. Select "System" if you want to use password feature every time the system boots up. The default setting is "Setup". You can create your password by using the "SUPERVISOR/USER PASSWORD" utility on the main program screen.

PCI/VGA Palette Snoop: The default setting is "Disabled". Set to "Enable" if any ISA adapetor card installed requires VGA palette snooping.

Video BIOS Shadow: The default setting is "Enabled" which will copy the VGA BIOS into system DRAM.

C8000-CBFFF Shadow to DC000-DFFFF Shadow: The default setting for the shadow feature is "Disabled". When enabled, the ROM with the specific address is copied into system DRAM. It will also reduce the size of memory available to the system.

PS/2 mouse function control: The Default setting is "Disabled". Set to "Enabled" when a PS/2 mouse is attached to the system and used as an input device.

OS Select For DRAM > 64MB: The default setting is "Non-OS2". Set to "OS2" if the system memory size is greater than 64MB and the operating system is OS/2.

After you have made your selection in the BIOS FEATURES SETUP, press the <ESC> key to go back to the main program screen.

3.10 CHIPSET FEATURES SETUP

Selecting “CHIPSET FEATURES SETUP” on the main program screen displays this menu:

Chipset Features Setup Screen

ROM PCI/ISA BIOS (2A59FF2A)
CHIPSET FEATURES SETUP
AWARD SOFTWARE, INC.

Auto Configuration	: Enabled	Chipset Special Features	: Enabled
DRAM Timing	: 70 ns		
DRAM RAS# Precharge Time	: 4	DRAM ECC/PARITY Select	: ECC
DRAM R/W Leadoff Timing	: 7/6	Memory Parity/ECC Check	: Auto
DRAM RAS To Cas Delay	: 3	Single Bit Error Report	: Disabled
DRAM Read Burst Timing	: x333/x444		
DRAM Write Burst Timing	: x333	Passive release	: Enabled
Turbo Read Leadoff	: Disabled	Delayed Transaction	: Disabled
DRAM Speculative Leadoff	: Disabled		
Turn-Around Insertion	: Disabled		
ISA Clock	: PCICLK/4		
System BIOS Cacheable	: Enabled		
Video BIOS Cacheable	: Enabled		
8 Bit I/O Recovery Time	: 1		
16 Bit I/O Recovery Time	: 1		
Memory Hole At 15M-16M	: Disabled		
Peer Concurrency	: Enabled		

ESC: Quit ↑↓→← :Select Item
F1 : Help PU/PD/+/-:Modify
F5 : Old Values (Shift) F2: Color
F6 : Load BIOS Defaults
F7 : Load Setup Defaults

This screen controls the settings for the board’s chipset. All the entries related to the DRAM timing and ISA clock on the screen are automatically configured. Do not make any change unless you are familiar with the chipset.

Auto Configuration: The default setting is “Enabled” which will set optimal DRAM timing automatically depending on whether the DRAM used is 70ns or 60ns. The other option is “Disabled” which allows you to change DRAM timing manually.

DRAM Timing: Choose DRAM speed 60ns or 70ns.

Memory Hole At 15M-16M: The default setting is "Disabled". Set to "Enabled" means that when the system memory size is equal to or greater than 16M bytes, the physical memory address from 15M to 16M will be passed to PCI or ISA and there will be 1MBytes hole in your system memory. This option is designed for some OS with special add-in cards which need 15M-16M memory space.

Peer Concurrency: The default setting is "Enabled" which allows CPU to run DRAM/External Cache cycles when PCI masters are running cycles targeting PCI peer devices. The other option is "Disabled".

Chipset Special Features: The default setting is "Enabled" which will enable all new 82430HX chipset features.

DRAM ECC/PARITY Select: There are two options: ECC or Parity, the default setting is ECC.

Memory Parity/ECC check: There are 2 options: Auto and Disabled. When set to "Auto", Parity or ECC check (depends on the setting of "DRAM ECC/PRITY Select") will be automatically enabled if SIMM modules with Parity bits are used.

Single Bit Error Report: If set to "Enabled", BIOS will report single bit error on the screen. The default setting is "Disabled".

Passive Release, Delayed Transaction: To enable the PCI Concurrency, these two options have to be set to "Enabled".

After you have made your selections in the CHIPSET FEATURES SETUP, press the <ESC> key to go back to the main program screen.

3.11 POWER MANAGEMENT SETUP

The "Power Management Setup" controls the mainboard's "Green" features.

Selecting "POWER MANAGEMENT SETUP" on the main program screen displays this menu:

Power Management Setup Screen

ROM PCI/ISA BIOS (2A59FF2A)
POWER MANAGEMENT SETUP
AWARD SOFTWARE, INC.

Power Management	:	Disable
PM Control by APM	:	No
Video Off Method	:	V/H SYNC+Blank
Doze Mode	:	Disable
Standby Mode	:	Disable
Suspend Mode	:	Disable
HDD Power Down	:	Disable

** Wake Up Events **

IRQ3 (Wake-Up Event)	:	OFF
IRQ4 (Wake-Up Event)	:	OFF
IRQ8 (Wake-Up Event)	:	OFF
IRQ12(Wake-Up Event)	:	OFF

** Power Down / Resume Events **

IRQ3 (COM 2)	:	OFF
IRQ4 (COM 1)	:	OFF

IRQ5 (LPT 2)	:	OFF
IRQ6 (Floppy Disk)	:	OFF
IRQ7 (LPT 1)	:	OFF
IRQ8 (RTC Alarm)	:	OFF
IRQ9 (IRQ2 Redir)	:	OFF
IRQ10 (Reserved)	:	OFF
IRQ11 (Reserved)	:	OFF
IRQ12 (PS/2 Mouse)	:	OFF
IRQ13 (Coprocessor)	:	OFF
IRQ14 (Hard Disk)	:	OFF
IRQ15 (Reserved)	:	OFF

ESC: Quit ↑↓→← :Select Item
F1 : Help PU/PD/+/-:Modify
F5 : Old Values (Shift) F2: Color
F6 : Load BIOS Defaults
F7 : Load Setup Defaults

Power Management: This setting controls the System Doze Mode, Standby Mode and Suspend Mode Timer features. There are four options:

User Define: Allows you to customize all power saving timer features.

Optimize: This is the recommended setting for general use.

Test/Demo: This is for test/demonstration purpose.

Disable: Disable the power management features.

PM Control by APM: The default setting is "No". If set to "Yes", system BIOS will wait for APM's prompt before it enters any PM mode.

Note: If your system power management is controlled by APM and there is a task running, the APM will not prompt the BIOS to enter any power saving mode after time out.

Video Off Method: This setting controls the Video off method in power saving mode. The default setting is "V/H SYNC+Blank" This setting disables V/H SYNC signals and blanks the screen in power saving mode. Other options are "Blank Screen" and "DPMS".

Doze Mode: Options are from "1 Min" to "1 Hour" and "Disable". The system speed will change from turbo to slow if no Power Management events occur for a specified length of time. Full power function will return when a Wake-Up event is detected.

Standby Mode: Options are from "1 Min" to "1 Hour" and "Disable". The system speed will change from turbo to slow and t he video signal will be suspended if no Power Management events occur for a specified length of time. Full power function will return when a Wake-Up event is detected.

Suspend Mode: Options are from "1 Min" to "1 Hour" and "Disable". The CPU clock will be stopped and the video signal will be suspended if no Power Management events occur for a specified length of time. Full power function will return when a Wake-Up event is detected.

HDD Power Down: Options are from "1 Min" to "15 Min" and "Disable". The IDE hard drive will spin down if it is not accessed within a specified length of time.

Wake-Up Events: When a hardware event is enabled, the occurrence of a corresponding event will return the system to full speed.

Power Down / Resume Events: when a hardware event is enabled, the occurrence of a corresponding event will prevent the system from entering any PM mode.

After you have made your selection in the POWER MANAGEMENT SETUP, press the <ESC> key to go back to the main program screen.

3.12 PNP / PCI CONFIGURATION

Both the ISA and PCI buses on the Mainboard use system IRQs & DMAs. You must set up the IRQ and DMA assignments correctly thru the PnP/PCI Configuration Setup utility, otherwise the Mainboard will not work properly.

Selecting "PNP / PCI CONFIGURATION" on the main program screen displays this menu:

PNP / PCI Configuration

ROM PCI/ISA BIOS (2A59FF2A)
PNP / PCI CONFIGURATION
AWARD SOFTWARE, INC.

Resources Controlled By	:	Manual	
Reset Configuration Data	:	Disabled	
IRQ-3 assigned to	:	Legacy ISA	
IRQ-4 assigned to	:	Legacy ISA	
IRQ-5 assigned to	:	PCI / ISA PnP	
IRQ-7 assigned to	:	Legacy ISA	
IRQ-9 assigned to	:	PCI / ISA PnP	
IRQ-10 assigned to	:	PCI / ISA PnP	
IRQ-11 assigned to	:	PCI / ISA PnP	
IRQ-12 assigned to	:	PCI / ISA PnP	
IRQ-14 assigned to	:	Legacy ISA	
IRQ-15 assigned to	:	Legacy ISA	
DMA-0 assigned to	:	PCI / ISA PnP	
DMA-1 assigned to	:	PCI / ISA PnP	
DMA-3 assigned to	:	PCI / ISA PnP	
DMA-5 assigned to	:	PCI / ISA PnP	
DMA-6 assigned to	:	PCI / ISA PnP	
DMA-7 assigned to	:	PCI / ISA PnP	

PCI IRQ Actived By	:	Level
PCI IDE IRQ Map To	:	PCI - AUTO
Primary IDE INT#	:	A
Secondary IDE INT#	:	B

ESC: Quit ↑ ↓ → ← :Select Item
F1 : Help PU/PD/+/-:Modify
F5 : Old Values (Shift) F2: Color
F6 : Load BIOS Defaults
F7 : Load Setup Defaults

Resources Controlled By: The defaults setting is “Auto” which will control all IRQs and DMAs automatically. The other option is “Manual” which allows you to control IRQs and DMAs individually.

Reset Configuration Data: The default setting is “Disabled”. When set to “Enabled”, The content of the ESCD block in flash BIOS will be cleared.

IRQ and DMA Assigned to.: If there is a legacy ISA device which uses an IRQ or a DMA, set the corresponding IRQ or DMA to “Legacy ISA”, otherwise you should set to PCI/ISA PnP.

PCI IRQ Actived By: Options are “Level” or “Edge”. The default setting is “Level”. This option is used to select the IRQ’s trigger method.

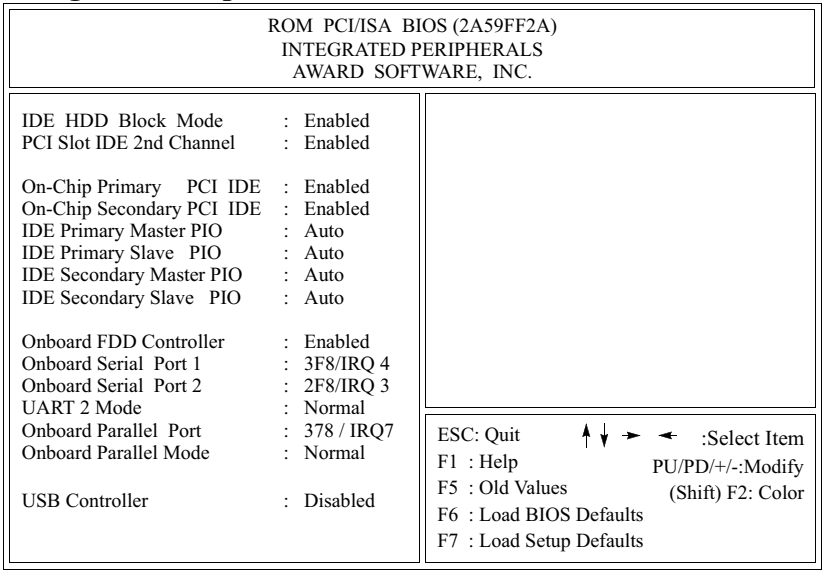
PCI IDE IRQ Map To, Primary IDE INT#, Secondary IDE INT#: If you disable onboard PCI IDE controller and install a PCI IDE card on the Mainboard, you need to set this option.If a PCI IDE Card which uses ISA IRQ directly thru a paddle card installed on an ISA slot, select “ISA” for the option “PCI IDE IRQ Map To”. If a PCI IDE Card uses PCI “INT” and is compliant to PCI Plug and Play specification, select “PCI-AUTO” for the option “PCI IDE IRQ Map To”. Otherwise select “PCI-SLOT n” (PCI-SLOT 1, PCI-SLOT 2 or PCI-SLOT 3) depends on which slot the PCI IDE Card is installed.

Only INT A and INT B are available for a PCI IDE Card, therefore you must set the PCI IDE Card’s primary interrupt to INT A and secondary interrupt to INT B. The INT A is routed to IRQ 14 and the INT B is routed to IRQ 15 thru a hardware router in the chipset.

3.13 INTEGRATED PERIPHERALS

Selecting “INTEGRATED PERIPHERIALS” on the main program screen displays this menu

Integrated Peripheral Screen



IDE HDD Block Mode: The Default setting is “Enabled”. This feature enhances hard disk performance by making multi-sector transfers instead of one sector per transfer. Most IDE drives, except very early design, have Block Mode transfer feature.

PCI Slot IDE 2nd Channel
The default setting is “Enabled”. This option enables the Secondary PCI IDE controller of the PCI IDE adapter.

On-Chip Primary/Secondary PCI IDE: The default setting is “Enabled”. This option enables the onboard Primary / Secondary PCI IDE controller.

IDE Primary Master PIO, IDE Primary Slave PIO, IDE Secondary Master PIO, IDE Secondary Slave PIO: There are six options "Auto", "Mode 0", "Mode 1", "Mode 2", "Mode 3" and "Mode 4". The default setting is "Auto". When set to "Auto" the BIOS will automatically set the mode to match the transfer rate of hard disk. If the system won't boot up when set to "Auto", set it manually to the lower mode. (e.g. From Mode 3 to Mode 2). All IDE drives should work with PIO mode 0.

Onboard FDD Controller: The default setting is "Enabled". This option enables the onboard FDD controller.

Onboard Serial Port 1 and Onboard Serial Port 2: These options are used to assign the I/O addresses for the two onboard serial ports. They can be assigned as follows:

3F8 / IRQ 4(Serial Port 1 default)
2F8 / IRQ 3(Serial Port 2 default)
3E8 / IRQ 4
2E8 / IRQ 3
Auto
Disabled (Disable the onboard serial port)

UART 2 Mode: Set this feature to IrDA, if an IrDA infrared module is used in the system.

Onboard Parallel Port: This option is used to assign the I/O address for the onboard parallel port. The options are "378/IRQ7" (defaults), "278/IRQ7", "3BC/IRQ7" and "Disabled" (disable the onboard parallel port). Note: Printer port always use IRQ7 when set "378/IRQ7" or "278/IRQ7" or "3BC/IRQ7" to "Enabled".

Onboard Parallel Mode: There are four options "Normal" (default) , "ECP", "ECP/EPP" and "EPP/SPP". Change the mode from "Normal" to the enhanced mode only if your peripheral device can support it.

ECP Mode Use DMA: When on-board parallel port set to ECP mode, the parallel port has option to use DMA "3"(default) or "1".

USB Controller: To activate the Universal Serial Bus function, this feature has to be set to "Enabled".

If you make any change for onboard FDD controller, serial ports or parallel port in this setup, save the change and turn off the system. After turning system on again the change will be effective.

3.14 SUPERVISOR / USER PASSWORD

The "SUPERVISOR/USER PASSWORD" utility sets the password. The Mainboard is shipped with the password disabled. If you want to change the password, you must first enter the current password, then at the prompt enter your new password. The password is case sensitive and you can use up to 8 alphanumeric characters, press <Enter> after entering the password. At the next prompt, confirm the new password by typing it and pressing <Enter> again.

To disable the password, press the <Enter> key instead of entering a new password when the "Enter Password" dialog box appears. A message will appear confirming that the password is disabled.

If you have set both supervisor and user password, only the supervisor password allows you to enter the BIOS SETUP PROGRAM.

Note:
If you forget your password, the only way to solve this problem is to discharge the CMOS memory by turning power off and placing a shunt on the JP2 to short pin 1 and pin 2 for 5 seconds, then removing the shunt.

4 Driver and Utility

4.1 Flash Utility

The BIOS of the 586F62T mainboard can be upgraded by using a Flash utility. A new version of the BIOS can be downloaded from the factory's BBS and Web site. Consult your vendor for the factory's BBS phone number and Web site address. The system BIOS is stored in a 1M-bit Flash EEPROM which can be erased and reprogrammed by the Flash utility.

There is a self-extracting archives file AWDFLASH.EXE. Execute the AWDFLASH.EXE to extract the following files.

FLASH.EXE	The Flash utility for AWARD BIOS upgrade.
README.TXT	A text file of instructions

The Flash utility will not work with any memory manager software running in the system. In order to make sure no memory manager software is running, boot your system from a bootable floppy disk which does not contain CONFIG.SYS nor AUTOEXEC.BAT files. If you are using MS-DOS 6.x, you can press <F5> function key while the “Starting MS-DOS...” appears on the screen to bypass the CONFIG.SYS and AUTOEXEC.BAT.

4.2 EIDE Bus Master Driver

The Bus Master EIDE logic designed in the Intel 82430VX chipset is intended to reduce the workload of the CPU and make the CPU running more efficiently. It will take care the data transfer between IDE drives and system memory and let CPU handle other tasks. In order to make the EIDE drive operate at bus-mastering DMA mode 2, the driver must be loaded properly.

There is a self-extracting archives file BMEIDE.EXE in the factory's BBS and Web site. Consult your vendor for the factory's BBS phone number and Web site address. Execute the BMEIDE.EXE to extract the following files.

BMIDE_95.EXE	Windows 95 archives
BMIDE_NT.EXE	Windows NT achieve
BMIDEOS2.EXE	OS/2 archives
README.TXT	A text file of instructions
LICENSE.TXT	A text file of license